

## A Design Technique To Reduce Nbti Effects From 5t Sram Cells

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### ABSTRACT

This paper focuses on designing an NBTI tolerant system by addressing the major reason of NBTI especially the devices that consists of SOC. To address this issue a thorough study of 5T SRAM cells has been done. This paper is based on idea of switch capacitors and the fact that only few transistors are ON at any particular time. RD model is primary and base model that us used to describe NBTI and aging degradation in this paper

The proposed technique improve read power by 8% and leakage power by 12.87%

**Keywords** – NBTI, 5T SRAM, AGING DEGRADATION, SWITCH CAPACITOR, SNM

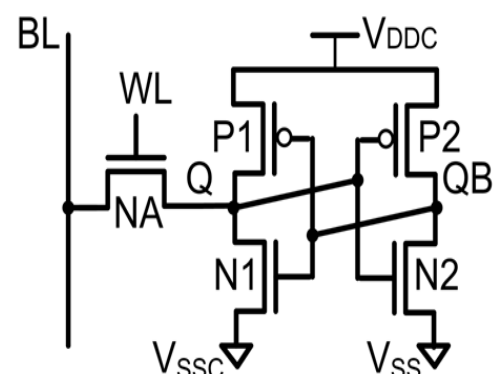
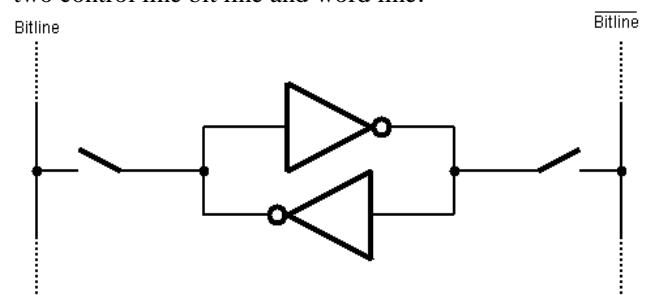
### I. INTRODUCTION

Any device is based on a pre-assumption or have a fault tolerance or error margin. So digital circuits do have a margin of about 15% in lifetime [2]. These margin are denoted by  $C_p^k$  numbers and there are several factors that governs this number and these factors are Hot Carrier Degradation, Gate Dielectric Breakdown and NBTI[7]. Among all of these NBTI is the most significant, because of two facts a) aging degradation i.e; older devices are more prone to failure b) Due to intense scaling that has been done after 1963[3]. Due to popularity of handheld devices in recent times the significance of SOC has been greatly increased since 90% of handheld devices come with SRAM. The major concern in today's devices are the computing unit and since these computing units depend on the amount of RAM, Cache Memory and thus the need for more and more is inevitable. Since SRAM consists of both PMOS and NMOS NBTI becomes a dominant factor in them as compared to DRAM. NBTI stands for Negative Bias Temperature Instability and is a phenomenon associated only with PMOS devices and happens when PMOS are stressed at elevated temperature with negative gate voltage. The effects on device characteristics are increased in threshold voltage and decrease in drive current, thus causing a reduction in speed.

### II. EVOLUTION OF SRAM

Static Random Access Memory are very significant part of SOC or CPU because speed on any CPU depends its SRAM. RAM in any CPU consists of both SRAMs and DRAMs and as SRAMs are faster than their counterpart DRAMs so the speed of any CPU majorly depends SRAMs But SRAMs comes with major drawbacks a) SRAMs are larger in size as compare to that of DRAMs b)

Presence of both PMOS and NMOS [9]. Fundamentally an SRAM consists of two back to back connected inverters. The output of first inverter is connected to the input of second and two pass transistors. These pass transistors control the cell operation of read and write Apart from this there are two control line bit line and word line.



During write cycle, access transistors are in ON state because of the fact that the data is placed on bit line and inverse data on inverse bit line then the access

transistors are turned on by applying word line due to which the transistor stores the value in it

During read cycle, pre charge is done to both bit line and inverse bit line and then the word line is enabled, due to this these word line the access transistor are enabled. The value stored are transferred to bit line leaving bit line to its pre charge value and discharge inverse bit line through N1 and N2 to logical 0. [1]

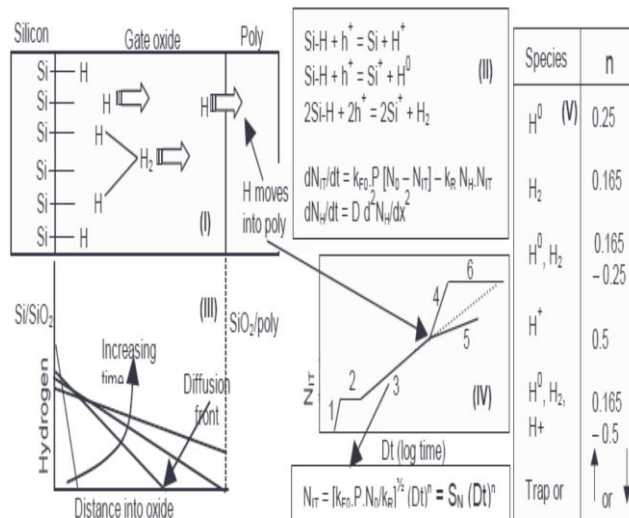
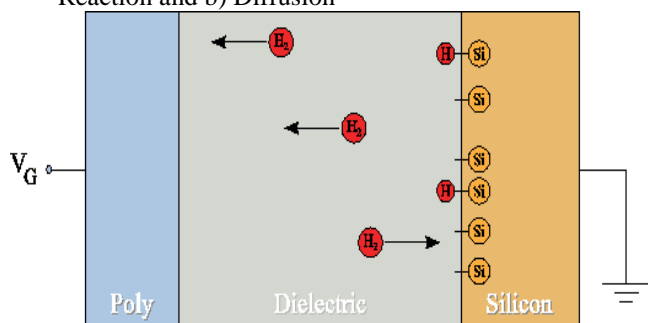
During standby operation the access transistors are in OFF state due to the fact that word line was not asserted. So the cross couple reinforces each and the data is stored as long as supply is maintained [4]

One of the biggest advantage of designing a digital circuit based on CMOS is that if we can change the channel length of a device we can increase or decrease the number of transistor in any circuitry [3]

The sole purpose of using two PTL is to overcome the static capacitance of back to back connected inverter pair. This can be simply done by using a proper sized 5T SRAM cells. Writing problem of SRAM cells can be overcome by using a proper sized access transistor. To enable write operation from 1 to 0 the ratio of width of pull up devices to that of access transistor should be smaller [8]. By decreasing the resistance of pull down transistor as compare to that of access transistor signal to noise margin can be improved. Increasing the width of pull down NMOS prevents the SRAM cell from being re written during read access and SNM can be improved. To provide high read stability the ratio of pull up and pull down transistors in first inverter is equal to 1 and in second its 1/6.15. [7]

### III. REACTION DIFFUSION MODEL

The reaction diffusion was first described in 1977 by JEPPSON and SVERSSON [7] and is one of most suitable method to describe NBTI and can be used to reproduce time evolution of device. As the name suggest this model has two parts a) Reaction and b) Diffusion



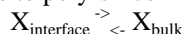
### 3a) Reaction



There is a field dependent electrochemical reaction at si-sio<sub>2</sub> interface these interfaces are electrically inactive. Since there are unstable Si at the interface hydrogen is passivated to form a Si-H bond. When the temperature increase these loosely formed bonds gets break which results in an interface trap (Nit).

### 3b) Diffusion

It states the transportation of H away from substrate to poly-silicon layer



There is also a reverse transportation in which hydrogen comes to bulk once again and forms the bond again [2]. The process at interface modelled by rate equation as

$$dN_{it}/dt = K_f(N_o - N_{it}(t)) - K_t N_{it}(t) N_x(0,t)^{1/a}$$

Where K<sub>f</sub> stands for interface trap, K<sub>t</sub> is rate of annealing Here, Si-H bonds breaks and capture a hole, leading to positively charged interface state and molecular hydrogen is formed [3]. At interface N<sub>x</sub>(0,t), the reaction i.e.; the forward reaction and backward reaction are controlled by hydrogen density. Since the hydrogen diffuse away from surface it degrades the quality of device and is given by

$$dN_x(x,t)/dt = D \nabla^2 N_x(x,t)$$

For each generated interface trap a hydrogen is released thus

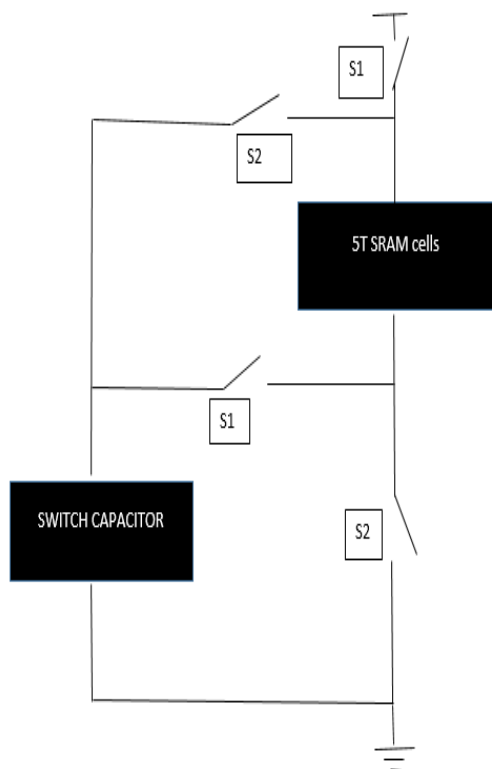
$$N_{it} = \int_2 N_x dx$$

### IV. PROPOSED TECHNIQUE

As the name suggests switch capacitor circuit consists of a switch and a capacitor and on the basis of on off state of switch, charges are stored in capacitors.

With the help of non-overlapping technique it can be assured that not all switches are ON at the same time. In a simple SRAM cell, the SRAM cell is directly connected from supply to ground. So during read and write cycle the charge will flow to the ground [9]

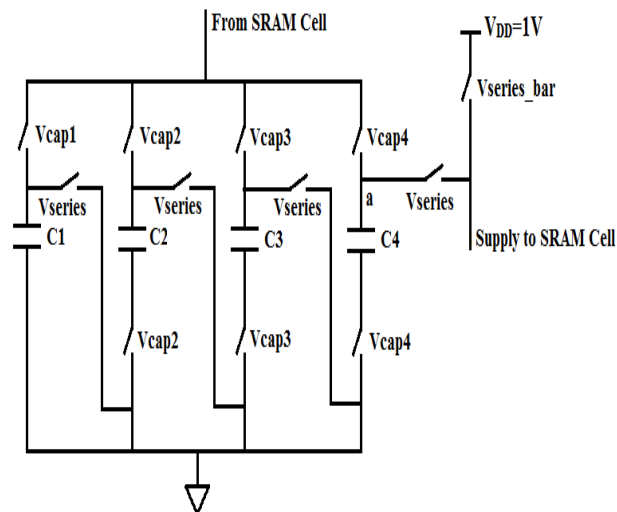
In the proposed technique switch capacitor will be placed between 5T SRAM cell and ground. So that the charge which was earlier getting wasted will now get stored in capacitor and once it meets with supply voltage value it will replace the supply voltage  $V_{dd}$  and will drive the SRAM cell.



There are basically two stages stage S1 and stage S2 during stage S1, the charge flows from SRAM cell and switch capacitor instead of directly going to the ground. Since the charge flows through switch capacitor the charge get stored in those capacitors. When the value of stored charge matches with that of the power supply then it can be replaced by supply voltage, thus saving power in the next phase of operation

In second stage S2, since the charge has been stored in stage S1 thus by switching to S2 it can drive the SRAM cell during idle state. Now in the idle state the SRAM is operating on voltage that is generated from the charge that would have been wasted in case switch capacitors were not used

#### 4.2 SWITCH CAPACITOR DESIGN



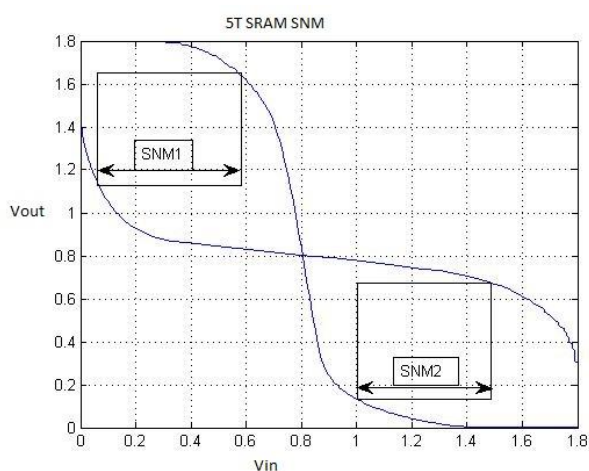
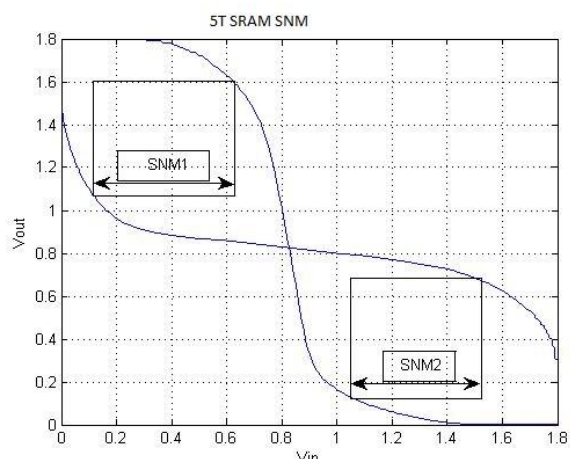
Initially  $V_{series}$  is in OFF state and  $V_{series\_bar}$  is in ON state. Now by switching to  $V_{cap}$  on, the read and write current depending in SRAM operation flows through SRAM cell which passes through the capacitor C1 resulting in rise in capacitor voltage up to 0.2V. When this capacitor reaches this value it gets turned off and the capacitor C2 gets switched ON this results in charging of C2 again when C2 reaches the value of 0.2 it gets switch off and in turn it switches C3 ON. When the fourth capacitor C4 gets fully charged i.e.; to 0.2 v  $V_{series}$  is turned ON resulting in connection of all capacitors in series thus adding the potential across each one of them. This results in total voltage off about 0.8v across node a. Now the switch capacitor is ready to drive the SRAM cells, so  $V_{series}$  is turned ON, the capacitor gets connected in series and now whenever the cell goes in idle state the switch capacitor will drive the cell instead of  $V_{dd}$ . Thus reducing the stand by power

#### V. RESULTS AND DISCUSSIONS

The simulations were done for 90nm technology with  $V_{dd} = 1.8$  v and the  $v_{th} = 0.36$ v. And an assumption has been made that there is about 10% of degradation in  $V_{th}$  when compared to NBTI to normal state [7].

##### 5.1 SNM

Signal to noise margin is defined as a maximum signal that can be accepted by any system without affecting the correct operation. In the proposed technique since the capacitors are added just before the ground so because of this the source potential of NMOS transistors gets increased [10] and because of this source biasing, the read margin gets reduced and thus it is better to check the stability of cell



According to above diagrams we can analyse that there is no significant reduction in SNM value when proposed technique is compared to that of conventional one. The results have been show in table 1

	WITHOUT NBTI	WITH NBTI
SNM	0.50v	0.42v

### 5.2 READ AND LEAKAGE

SRAM	VOLTAGE (v)	READ (uA)	LEAKAGE (uA)
CONVENTIONAL 5T SRAM CELL	1.8v	418uA	101uA
PROPOSED TECHNIQUE	1.8v	402uA	88uA
IMPROVEMENT (%)		8%	12.87%

Table 2 shows read and leakage power comparison of conventional and proposed technique. The supply voltage is maintained at 1.8V. The threshold voltage Vth without NBTI is 0.36v and with NBTI its 0.33. So by comparing the the conventional technique with the proposed one it shows around 8%

improvement on read power and around 12.87% improvement on leakage power

### VI. CONCLUSION

NBTI has been always a major concern in silicon industry esp. after the intense scaling that took place after 1960s. A close review of literature suggests that there are two phases in NBTI pre 2003 and post 2003. Pre 2003 shows a degradation in which the time exponent and temperature activation are not consistent whereas post 2003 leads us to a very simplified view of NBTI i.e.; NBTI is an interface trap driven phenomenon which occurs because of breaking of loosely bonded Si-H when applied to elevated temperature [5].

A 5T SRAM cell with switch capacitor technique was proposed in this research work. And after the several analysis the result indicates a significant amount of reduction of overall power. It can be seen from results that around 12.87% improvement on leakage power and around 8% improvement on read power. It is also been shown that there is no significant change on SNM value of 5T SRAM cell. The idea is that if the stress get reduce on SRAM cell the rate of Vth degradation also gets reduce. Since a switch capacitor circuit has been added between 5T SRAM cell and ground during the normal state the capacitor gets charged and the source potential of SRAM gets increased thus it reduces the stress on both PMOS devices and when the switch capacitor gets sufficiently charged they can be used to drive the circuit thus reduces the power consumption of device. Hence the proposed SRAM cell is suitable for low power approach on handheld devices

### REFERENCES

- [1] Rencho Raju Thomas, 2004. Technische Universität München. .
- [2] M.A. ALAM, H. Kufuoglu, D. Varghese and S Mahapatra, . 2006 A comprehensive model for PMOS NBTI degradation .Purdue University, West Lafayette, USA.
- [3] Deal BE, Skalar M, Grove AS. Characteristics of surface state charge (Qss) of thermally oxidized silicon j electrochem SOC 1973;120:90
- [4] Strain RJ, Goetzberger A, Snow EH, characteristics of surface state during stress aging of thermal Si-SiO2 interfaces J Electrochem SOC 1973
- [5] M A Alam,S Mahapatra, A comprehensive model of PMOS NBTI degradation,Agere system Allentown,USA,2004
- [6] Tony Tae-Hyoung Kim and Zhi Hui Kong, Impact analysis of NBTI/PBTI on SRAM Vmin and a design technique to improve the SRAM Vmin, JOURNAL OF

SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.13, NO.2, APRIL, 2013

- [7] Kaushik Roy, Kufluglu H, M A ALAM, Impact of NBTI on nano scale SRAM array: modeling and analysis, IEEE council in Electronics design automation,
- [8] Wenping wang, Shengpi Yang Sarvesh Bhardwaj, Department of electrical engineering, Arizona state university Tempe, USA, 2009. Taniya Siddiqua and sudhavana Gurumurthi, Recovery boosting: A technique to enhance NBTI recovery in SRAM Arrays, Department of computer science, University of Virginia
- [9] Ming-chao lee, Yu Guang Chen, Ding kei Huang, NBTI Aware power gating design, Department of CS, National Tsing hua University, Hsinchu Taiwan
- [10] Sauvik Mahapatra, Dipankar saha, Dhanoop Vargese, On the generation and recovery of interface trap in MOSFET subjected to NBTI, FSI, IEEE, 2006
- [11] M Bagatin, S gerardin, A Paccagnella Does NBTI affect soft error rate in SRAM, React group, university di Padova Italy
- [12] Sayab Khan, said Hamdioui, Trends and challenges of SRAM reliability in Nanoscale era, Delft university of technology, IEEE, 2010
- [13] Sanjay V kumar, Chris H Kim and Sachin S Sapatnkar, Impact of NBTI on SRAM read stability and design for reliability, University of Minnesota, Minneapolis, 2005
- [14] Asen Asenov, Andrew R Brown and Binjie cheng, Statistical aspects of NBTI/PBTI and impact on SRAM yield, Gold standard simulation ltd, School of engineering, University of Glasgow, UK